

We claim:

- 1 1. A method in the fabrication of an integrated circuit including at least one bipolar
2 transistor and at least one MOS device comprising the steps of:
3 - providing a silicon substrate;
4 - forming an active region for the bipolar transistor and an active region for the MOS
5 device in said silicon substrate;
6 - forming field isolation areas around, in a horizontal plane, said active regions;
7 - forming a MOS gate region on said active region for the MOS device;
8 - forming a layer of an electrically insulating material on said MOS gate region and on
9 said active region for the bipolar transistor; and
10 - defining a base region in said active region for the bipolar transistor by means of
11 producing an opening in said electrically insulating layer, wherein
12 - said opening in said electrically insulating layer is produced so that the remaining
13 portions of the electrically insulating layer partly cover said active region for the bipolar
14 transistor; and
15 - said electrically insulating layer remains on said MOS gate region to encapsulate and
16 protect the MOS gate region during subsequent manufacturing steps.
- 1 2. The method as claimed in claim 1 wherein said electrically insulating layer is a
2 nitride layer.
- 1 3. The method as claimed in claim 1 further comprising the step of manufacturing
2 of a capacitor, wherein a portion of said electrically insulating layer is utilized as the
3 dielectric in said capacitor.
- 1 4. The method as claimed in claim 1 wherein said MOS gate region is formed as a
2 silicon layer on top of an oxide layer.

1 5. The method as claimed in claim 4 wherein an oxide is formed on top of the
2 silicon layer prior to forming said electrically insulating layer.

1 6. The method as claimed in claim 4 further comprising the step of forming an
2 oxide layer on top of said active region for the bipolar transistor prior to forming said
3 electrically insulating layer.

1 7. The method as claimed in claim 6 further comprising the step of producing said
2 opening also through said oxide layer on top of said active region so as to expose a
3 portion of said active region for the bipolar transistor.

1 8. The method as claimed in claim 6 wherein said oxide layer, on top of which said
2 gate polysilicon layer is formed, and said oxide layer formed on top of said active region
3 for the bipolar transistor are formed simultaneously.

1 9. The method as claimed in claim 1 wherein said active region for the MOS device
2 is ion implanted prior to the formation of said MOS gate region.

1 10. The method as claimed in claim 1 wherein a secondary implanted collector in
2 said active region for the bipolar transistor and a background doping of said active region
3 for the MOS device are formed simultaneously in an ion implantation step.

1 11. The method as claimed in claim 10 wherein an extrinsic base for the bipolar
2 transistor is formed on said electrically insulating layer and partly on said active region
3 for the bipolar transistor in said opening to thereby define an emitter opening, said
4 extrinsic base being formed prior to said ion implantation step and being protected by
5 photoresist during said ion implantation step.

1 12. The method as claimed in claim 11 wherein said extrinsic base is doped and
2 source and drain regions are formed in said active region for the MOS device
3 simultaneously in an ion implantation step.

1 13. The method as claimed in claim 12 wherein also an electrode of a capacitor or a
2 contact layer for a substrate contact is doped in the ion implantation step, in which said
3 extrinsic base is doped.

1 14. The method as claimed in claim 12 wherein a silicon oxide and silicon nitride bi-
2 layer is formed on said doped source and drain regions to thereby prevent implanted
3 species from diffusing out of said active region.

1 15. The method as claimed in claim 1 wherein said active regions for the bipolar
2 transistor and the MOS device are formed by means of ion implantation through an
3 oxide-nitride bi-layer.

1 16. The method as claimed in claim 1 wherein a collector including a collector
2 plug for said bipolar transistor is formed, and wherein said collector plug is doped by
3 means of ion implantation with two different dopant species of the same doping type,
4 but which have different diffusivities, so as to achieve a low-resistive and deep
5 collector plug.

1 17. The method as claimed in claim 16 wherein an emitter contact is formed, and
2 wherein said emitter contact is doped with one of said dopant species used in said
3 collector plug implantation.

1 18. The method as claimed in claim 16 wherein said ion implantation of the collector
2 plug is performed in three separate steps, each step comprising the ion implantation of a
3 dopant species at a set energy and a set dose.

1 19. The method as claimed in claim 18 wherein high resistance and low resistance
2 resistors are formed in said three-step ion implantation.

1 20. The method as claimed in claim 1 wherein the bipolar transistor is an NPN-
2 transistor and the MOS device is a PMOS transistor.

- 1 21. The method as claimed in claim 1 further comprising the steps of:
2 - forming a buried collector region for the bipolar transistor in said substrate, said buried
3 collector region being located underneath said active region for the bipolar transistor;
4 - producing the field isolation area formed around the active region for the bipolar
5 transistor as a shallow trench in said silicon substrate, said shallow trench extending
6 vertically from the substrate surface and down into the buried collector region; and
7 - filling said shallow trench with an electrically insulating material.
- 1 22. The method as claimed in claim 21 wherein said buried collector region and
2 said shallow trench are formed relative each other so that said buried collector region
3 extends into areas located underneath said shallow trench.
- 1 23. The method as claimed in claim 22 wherein said buried collector region is
2 strongly n-doped.
- 1 24. The method as claimed in claim 21 wherein a deep trench is formed in said
2 shallow trench.
- 1 25. The method as claimed in claim 1 wherein a vertical bipolar transistor is
2 formed in said active region for the bipolar transistor, the doping profiles and heat
3 treatment thereof being designed to produce a transistor, which will fully deplete from
4 its base to its subcollector at a base-collector bias voltage larger than 2 V.
- 1 26. The method as claimed in claim 1 wherein a vertical bipolar transistor is
2 formed in said active region for the bipolar transistor, the doping profiles and heat
3 treatment thereof being designed to produce a transistor, which will fully deplete from
4 its base to its subcollector at a base-collector bias voltage larger than 1 V.
- 1 27. The method as claimed in claim 25 wherein the collector is formed with a
2 retrograde doping profile.

1 28. The method as claimed in claim 1 wherein said integrated circuit is an
2 integrated circuit for radio frequency applications.

1 29. The method as claimed in claim 1 wherein said subsequent manufacturing
2 steps include a step of oxidation, ion implantation, or etching.

1 30. The method as claimed in claim 8 wherein said oxide layer, on top of which
2 said gate polysilicon layer is formed, and said oxide layer on top of said active region
3 for the bipolar transistor are grown.

1 31. The method as claimed in claim 23 wherein said buried collector region is n-
2 doped to a concentration of at least about $1\text{E}19\text{ cm}^{-3}$.

1 32. The method as claimed in claim 23 wherein said active region for the bipolar
2 transistor is doped to a concentration not higher than about $1\text{E}17\text{ cm}^{-3}$.

1 33. The method as claimed in claim 23 wherein said active region for the bipolar
2 transistor is doped to a concentration not higher than about $1\text{E}16\text{ cm}^{-3}$.

1 34. The method as claimed in claim 23 wherein said active region for the bipolar
2 transistor is doped to a concentration of about $1\text{E}16\text{ cm}^{-3}$.

1 35. The method as claimed in claim 24 wherein said deep trench is self-aligned to
2 said shallow trench.

1 36. In the fabrication of an integrated circuit, a method for forming a shallow trench
2 for isolation of a vertical bipolar transistor comprised in said circuit, comprising the steps
3 of:
4 - providing a semiconductor substrate of a first doping type;
5 - forming a buried collector region of a second doping type for the bipolar transistor in
6 said substrate;
7 - epitaxially growing a silicon layer on top of said substrate;
8 - forming an active region of said second doping type for the bipolar transistor in said
9 epitaxially grown silicon layer, the active region being located above the buried collector
10 region;
11 - forming a shallow trench in said epitaxially grown silicon layer and said silicon
12 substrate, said shallow trench surrounding, in a horizontal plane, said active region and
13 extending vertically a distance into said substrate; and
14 - filling said shallow trench with an electrically insulating material.

1 37. The method as claimed in claim 36 wherein said buried collector region and
2 said shallow trench are formed relative each other so that said buried collector region
3 extends into areas located underneath said shallow trench.

1 38. The method as claimed in claim 36 wherein said shallow trench is formed by
2 means of masking and etching.

1 39. The method as claimed in claim 36 wherein said substrate doping is of p-type
2 and said buried collector region and said active region dopings are of n-type.

1 40. The method as claimed in claim 39 wherein said buried collector region is
2 strongly n-doped.

1 41. The method as claimed in claim 36 wherein a deep trench is formed in said
2 shallow trench.

1 42. The method as claimed in claim 36 wherein said integrated circuit is an
2 integrated circuit for radio frequency applications.

1 43. The method as claimed in claim 40 wherein said buried collector region is
2 doped to a concentration of at least about $1\text{E}19\text{ cm}^{-3}$.

1 44. The method as claimed in claim 40 wherein said active region is doped to a
2 concentration not higher than about $1\text{E}17\text{ cm}^{-3}$.

1 45. The method as claimed in claim 40 wherein said active region for the bipolar
2 transistor is doped to a concentration not higher than about $1\text{E}16\text{ cm}^{-3}$.

1 46. The method as claimed in claim 40 wherein said active region for the bipolar
2 transistor is doped to a concentration of about $1\text{E}16\text{ cm}^{-3}$.

1 47. The method as claimed in claim 41 wherein said deep trench is self-aligned to
2 said shallow trench.

1 48. An integrated circuit comprising:
2 - a semiconductor substrate of a first doping type, said substrate having an upper surface;
3 - a vertical bipolar transistor formed in said substrate, the transistor including an active
4 region of a second doping type, wherein an emitter and a base are formed, and a buried
5 collector region of said second doping type, said buried collector region being located
6 underneath the active region; and
7 - a shallow trench for isolation of the vertical bipolar transistor, wherein said shallow
8 trench surrounds, as seen along the surface of the substrate, the active region of said
9 transistor, and is filled with an electrically insulating material, wherein
10 - said shallow trench extends vertically from the upper surface of the substrate and
11 down into the substrate to a depth where said buried collector region is located.

1 49. The integrated circuit as claimed in claim 48 wherein said buried collector
2 region extends into areas located underneath said shallow trench.

1 50. The integrated circuit as claimed in claim 48 wherein said buried collector
2 region is strongly n-doped.

1 51. The integrated circuit as claimed in claim 48 wherein said integrated circuit is
2 adapted for radio frequency applications.

1 52. The integrated circuit as claimed in claim 50 wherein said buried collector
2 region is doped to a concentration of at least about $1\text{E}19\text{ cm}^{-3}$.

1 53. The integrated circuit as claimed in claim 50 wherein said active region is
2 doped to a concentration not higher than about $1\text{E}17\text{ cm}^{-3}$.

1 54. The integrated circuit as claimed in claim 50 wherein said active region is
2 doped to a concentration not higher than about $1\text{E}16\text{ cm}^{-3}$.

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- 1 55. The integrated circuit as claimed in claim 50 wherein said active region is doped
- 2 to a concentration of about $1\text{E}16\text{ cm}^{-3}$.